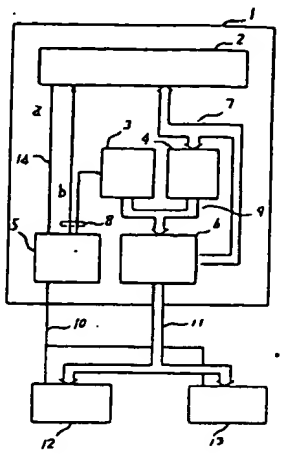
(54) AUTOMATIC SCANNING SY[redacted]
(11) 63-254553 (A) (43) 21.10.[redacted]19) JP
(21) Appl. No. 62-88041 (22) 10.4.1987
(71) NEC CORP(2) (72) SHINICHI MANABE(3)
(51) Int. Cl⁴. G06F15/16

PURPOSE: To scan slave processors under the control of a main processor without any waste by storing slave processor addresses to be scanned in all areas to be accessed by a counter and sending out the output data of the memory to the slave processors as the slave processor addresses.

CONSTITUTION: The main processor 1 has a microprocessor 2 which performs principal processing, a processing request detection part 5 which sends out a driving signal at specific time-limit intervals by being driven by the microprocessor 2 and stopping the transmission of the driving signal on receiving a processing request from a slave processor 12 or 13 and also outputs a processing request signal to the microprocessor 2, a counter 3 which receives the driving signal, counts up, and outputs its counted value, and a memory part 6 which stores addresses of the slave processors 12 and 13 to be scanned in all storage areas to be looked up with all counted values outputted by the counted by the counter 3 and outputs addresses to the slave processors 12 and 13 according to the counted values. Consequently, response to the slave processors 12 and 13 is speeded up.

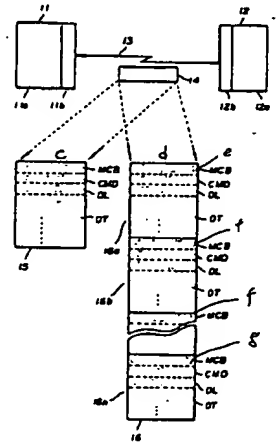


5: processing request detection part, 6: memory part, 7: data bus, 8: scan control line, 9: memory address, 10: scan response line, 11: address bus, a: driving line, b: processing request signal

(54) DATA TRANSFER SYSTEM
(11) 63-254554 (A) (43) 21.10.1988 (19) JP
(21) Appl. No. 62-88413 (22) 10.4.1987
(71) FANUC LTD (72) MAKI SEKI(2)
(51) Int. Cl⁴. G06F15/16,G06F13/38

PURPOSE: To obtain a data transfer system which requires only a small-capacity buffer by discriminating the head, middle, and tail of a data block in split transfer mode according to control data and composing a group of significant data, and performing specific processing according to a command and the data.

CONSTITUTION: A 1st processor unit 11 discriminates between a batch transfer mode and the split transfer mode and transfers control data MCB indicating that the data block is the head, middle, or tail to a 2nd processor unit 12 in split transfer mode together with a command and data. Then, the 2nd processor unit 12 performs processing according to the received command and data in batch transfer mode. In split transfer mode, on the other hand, the head, middle, and tail are discriminated according to the control data MCB to compose the group of significant data and specific processing is carried out according to the command and data. Consequently, only the small-capacity buffer is required.



11b: communication interface, 12a: subprocessor, 12b: communication interface, CMD: command, DL: data length, DT: data, c: batch transfer mode, d: split transfer mode, e: head, f: middle, g: tail

(54) SHARED DUAL MEMORY CONTROL SYSTEM
(11) 63-254555 (A) (43) 21.10.1988 (19) JP
(21) Appl. No. 62-88822 (22) 13.4.1987
(71) HITACHI LTD (72) YOSHIHIRO MIYAZAKI(3)
(51) Int. Cl⁴. G06F15/16

PURPOSE: To evade a system stop by accessing a system area where writing to the same address is performed in conflict by using a synchronous type selecting device normally, but an independent type selecting device in the case of the fault of the synchronous type selecting device.

CONSTITUTION: The independent type selecting device 15 which performs selection control independently of other shared memories and the synchronous type selecting device 16 where a slave system memory selects a CPU according to the selection result of a master system memory are provided in a shared memory 1a; and the former 15 is used normally for access to a user area and the latter 16 is used for access to a system area. When the latter 16 is in trouble, other CPUs are inhibited from accessing the system area through an inter-CPU linkage mechanism provided separately with the system program of a CPU determined as a master previously and then the independent selecting device 15 is used to access the system area and carry on processing. Consequently, the synchronizing type selecting device 16 does not becomes a bottle neck of the reliability of the whole system and high system reliability is obtained.